ABSTRACT OF THE DISCLOSURE

In a semiconductor device in which a wiring layer having an area which overlaps a connecting position and a wiring layer having an area which does not overlap the connecting position exist, if the wiring layer having the area which overlaps the connecting position is formed by connecting exposure, a pattern is formed in consideration of an alignment margin. Therefore, it is not advantageous in terms of a wiring width and a space between the wirings as compared with those in the case of forming the wiring layer by a batch processing of exposure. In a manufacturing method of a semiconductor device having a plurality of wiring layers, a first wiring layer is formed as a pattern by dividing a desired pattern into a plurality of patterns, connecting the divided patterns, and exposing them, and a second wiring layer is formed, as a pattern, by the batch processing of exposure.